INFRASTRUCTURE FOR AVF MODELING

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OVERVIEW

AMD

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- Architectural Vulnerability Factors
  - Program Vulnerability Factor
  - Hardware Vulnerability Factor
  - Spatial Multi-bit Architectural Vulnerability Factor
- Infrastructure for AVF Measurement
  - Infrastructure Overview
  - API Overview

MOTIVATION

MICROPROCESSOR RELIABILITY AND TRANSIENT FAULTS

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- Reliability is a major constraint in the design of microprocessors
- Transient faults are a primary concern in designing reliable microprocessors
  - These faults occur when a particle strike deposits enough charge to flip state in storage elements
- Microprocessor vendors set a failure rate (FIT) target and perform significant analysis to efficiently design for and validate against this target
  - Pre-RTL
    - Architectural Vulnerability Analysis
  - Pre-Silicon
    - Statistical Fault Injection
  - Post-Silicon
    - Particle Beam Testing

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Architectural Vulnerability Factors

ARCHITECTURAL VULNERABILITY FACTORS (AVF)
[MUKHERJEE03]

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- Not all faults (bit flips) become errors (incorrect program output)
- The Architectural Vulnerability Factor (AVF) of a hardware structure is defined as the probability that a fault in the structure becomes an error
- AVF can be conservatively estimated through ACE Analysis
  - Determines during each cycle which bits are required for Architecturally Correct Execution (ACE)

$$AVF_H = \frac{\sum_{n=0}^{N} ACE\ bits\ in\ H\ at\ cycle\ n}{B_H \times N}$$

B_H: Size in bits
N: Number of cycles

  - Multiple variants of AVF for multiple structures can be estimated during a single fault-free simulation run
  - Well suited to early stage (pre-RTL) design exploration
  - Much faster than software fault injection

ARCHITECTURAL VULNERABILITY FACTORS CONT.

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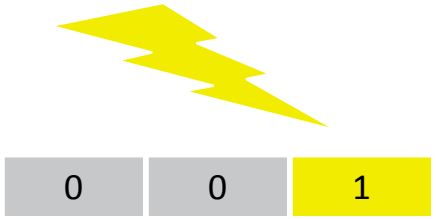
HARDWARE VULNERABILITY FACTORS AND PROGRAM VULNERABILITY FACTORS [SRIDHARAN09, SRIDHARAN10]

- Faults which do not propagate into errors are called masked
- Faults can become masked at many different levels in a system
  - Device level masking
    - Circuit level timing
  - Microarchitecture level masking (Hardware Vulnerability Factor)
    - Register lifetimes
    - Performance enhancing state (branch prediction tables)
  - Architecture level masking (Program Vulnerability Factor)
    - Dynamically dead state
    - Logically masked state
  - Application level masking
    - Approximately correct state
- AVF considers both microarchitectural and architectural masking
  - AVF = HVF x PVF

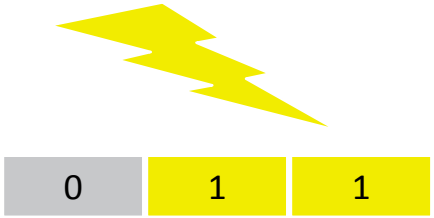
ARCHITECTURAL VULNERABILITY FACTORS CONT.

SPATIAL MULTI-BIT ARCHITECTURAL VULNERABILITY FACTORS [WILKENING14]

- As process technology scales downward it becomes more likely a single particle strike will simultaneously flip multiple bits
  - This is known as a spatial multi-bit transient fault
- The effects of spatial multi-bit faults are non-trivial, and spatial multi-bit AVF (MBAVF) can vary significantly from single-bit AVF
- MBAVF can give insight into reliability behavior involving
  - Various multi-bit patterns (fault modes)
  - Different interleaving schemes and error correcting codes
  - Both microarchitectural and architectural masking



Single-bit Fault



Multi-bit Fault

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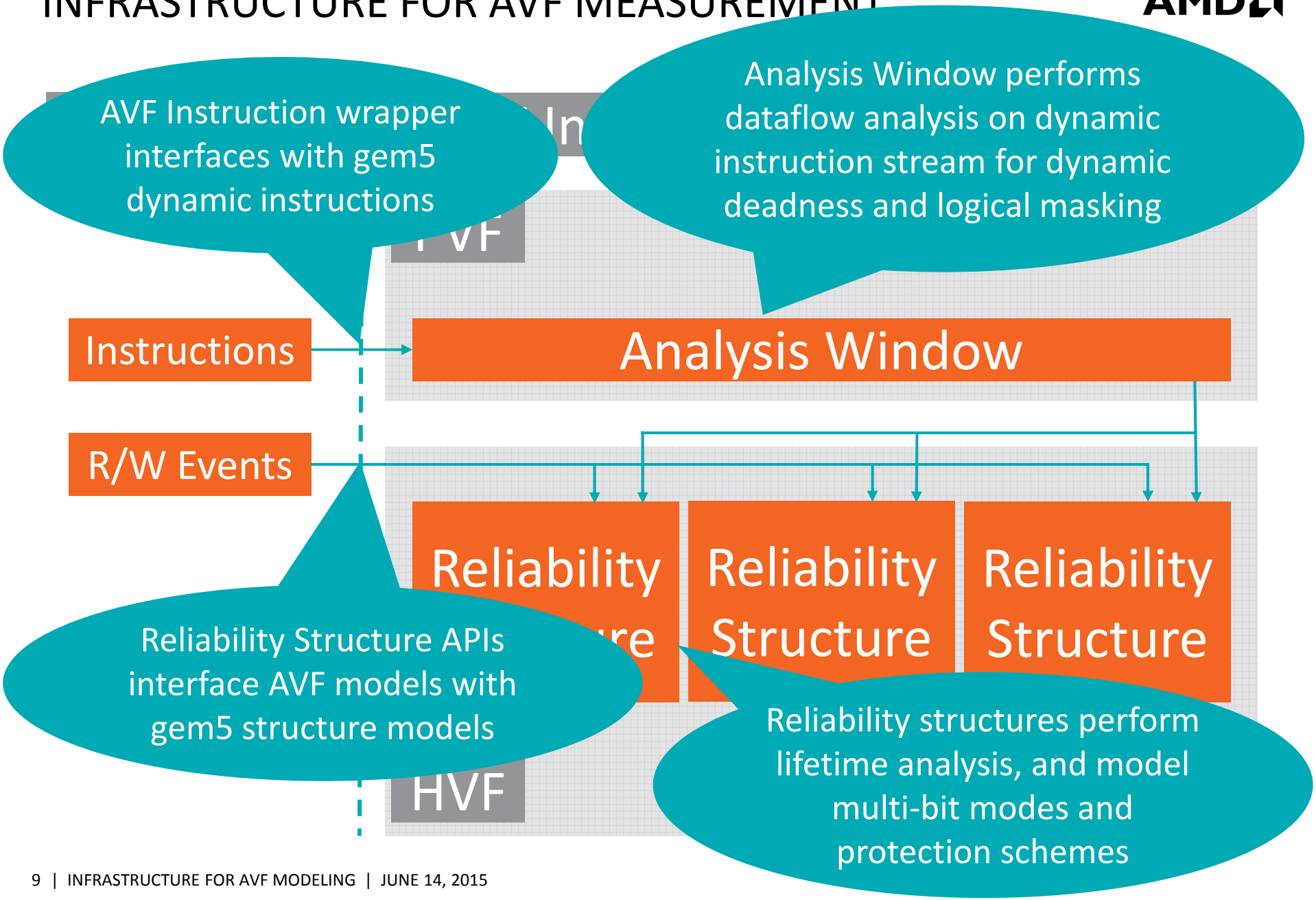
Infrastructure for AVF Measurement

INFRASTRUCTURE FOR AVF MEASUREMENT



INFRASTRUCTURE FOR AVF MEASUREMENT

API OVERVIEW

- Register committed instructions
  - PostCommitBuffer->insert(

```
instruction,                                  // dynamic instruction
curTick())                                    // commit cycle
```

- Register read and write events to modeled state
  - Pass cycle, identifying information for associated instruction, location in modeled structure, and associated architectural state
  - CPURegisterFile->read_with_association(

```
curTick(),                                    // current cycle
device_id, context_id, thread_id, dynamic_id, // instruction identifiers
2, true, 3,                                   // info needed for variable length arguments
reg_num, byte,                                // register #, byte – physical register location
thread_id, reg_num, byte)                     // thread, register #, byte – architectural state
```

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Questions?

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