DRAM Power-Down States in gem5

gem5 workshop at Arm Research Summit

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Background - DRAM in gem5

System Interconnect

Memory Controller

DRAM Power

DRAM DIMM

Request

Response

Command

Data

Defined specifications
- JEDEC
- DRAM manufacturers

Currents, voltages

Energy = f(command, Xme, currents, voltages)

JEDEC DRAM manufacturers

Defined specifications
Memory controller function

JEDEC defined states
- Active
- Idle
- Active Power-Down
- Precharge Power-Down
- Self-Refresh

Controller designers implement their own power state entry and exit control

Reference for gem5 DRAM controller:

Code committed, paper in MEMSYS Conference ‘17
Scheduling power-down (PD) state transitions

Conditions to enter power-down state

Enter power-down (PD) state if:
- There are no requests in the queue AND
- There are no pending events

Which PD state depends on:
- At least one bank open -> Active PD (PDNA)
- All banks closed -> Precharge PD (PDNP)
- Previous state was Precharge PD -> enter Self-Refresh (SREF)

Staggered power-down strategy

Do the PD modes work? What is their impact?

Breakdown of energy per state

Closed adaptive page policy

Open adaptive page policy

Performance / energy trade-off

Impact of low power modes

% Increase in Time  % Energy Saving

Memory part is based on 2 rank Micron DDR4-2400 8 Gbit datasheet
Modeling details and validation results in MEMSYS ‘17 paper

DRAM is a major energy consumer and DRAM power-down modes are now integrated to enable richer full-system energy-efficiency studies

Integrating DRAM Power-Down Modes in gem5 and Quantifying their Impact

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Thank You!
Danke!
Merci!
谢谢!
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Gracias!
Kiitos!
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